TOPTOP "TS2926"

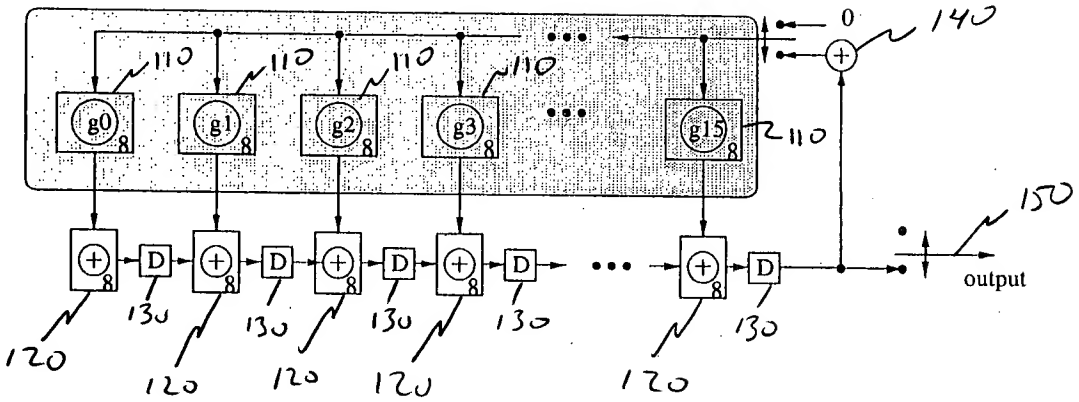


FIG. 1 (PRIOR ART)

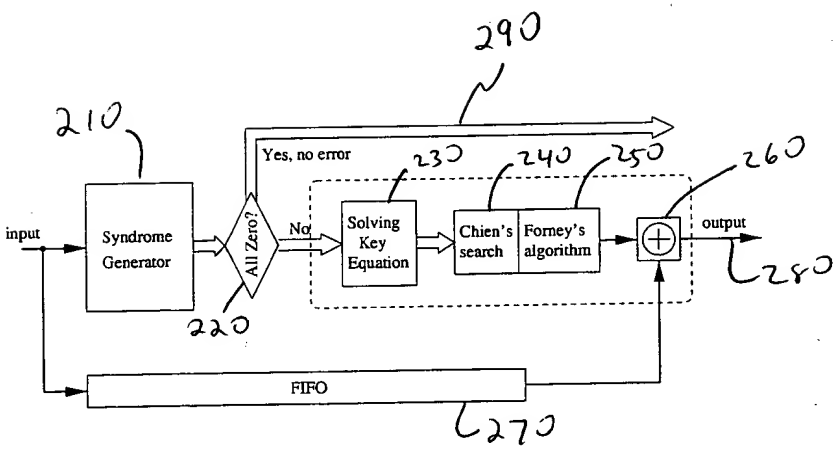


FIG. 2 (PRIOR ART)

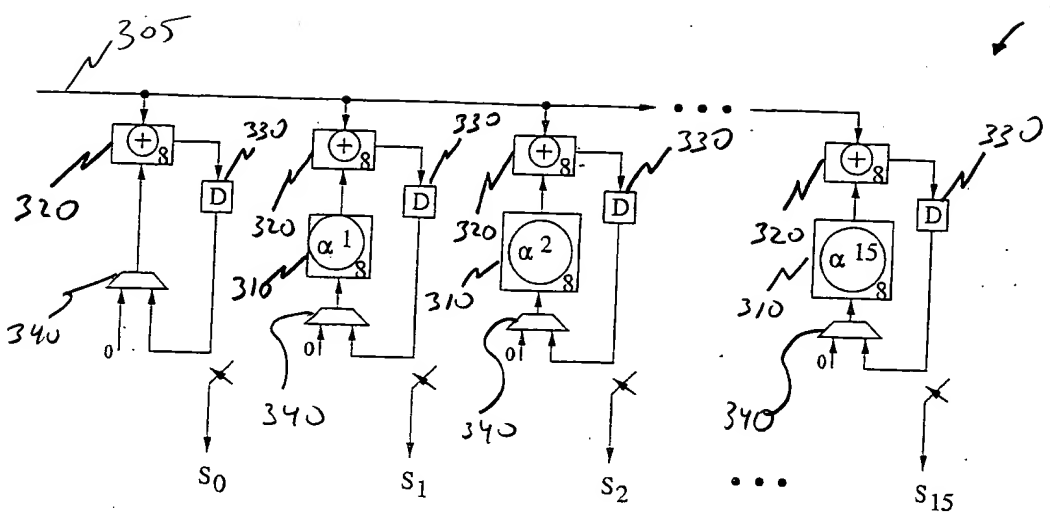


FIG. 3 (PRIOR ART)

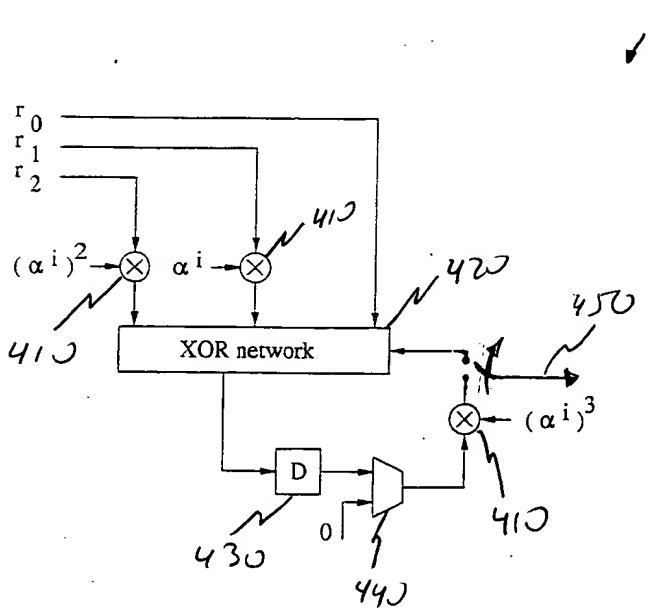


FIG. 4

500

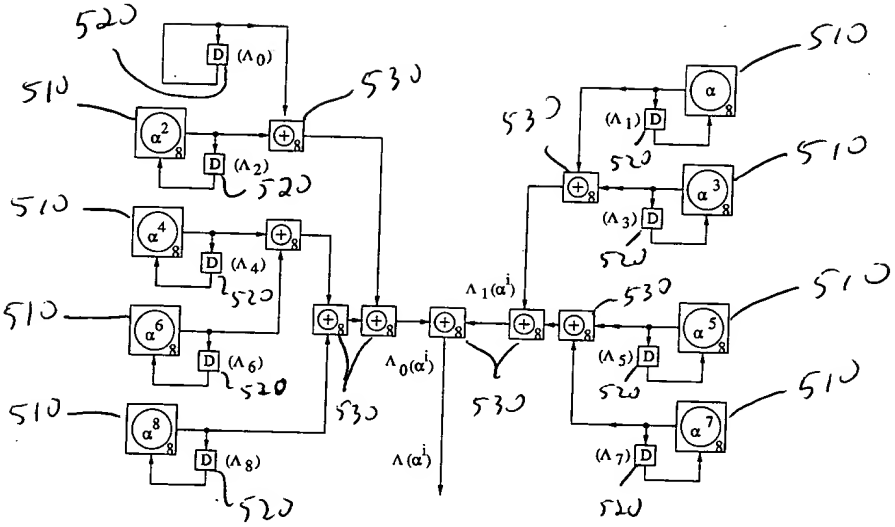


FIG. 5 (PRIOR ART)

600

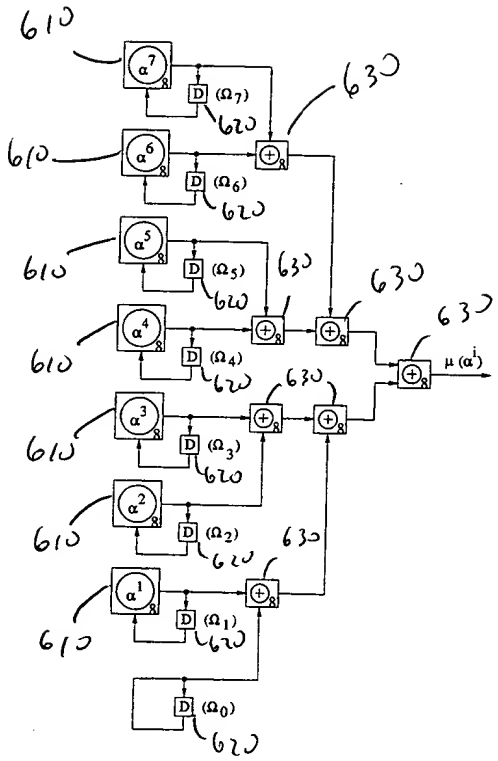


FIG. 6 (PRIOR ART)

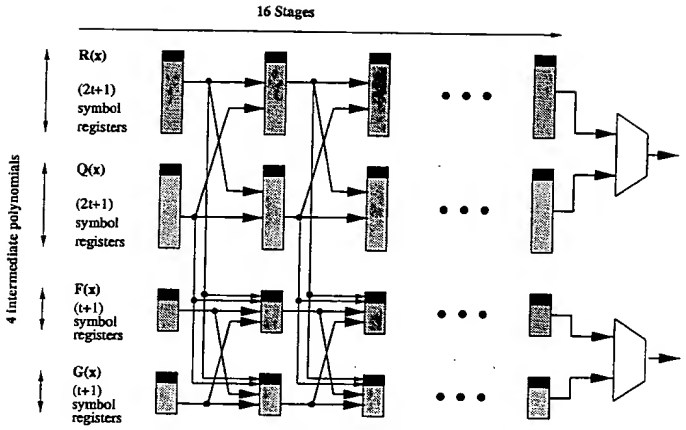


FIG. 7 (PRIOR ART)

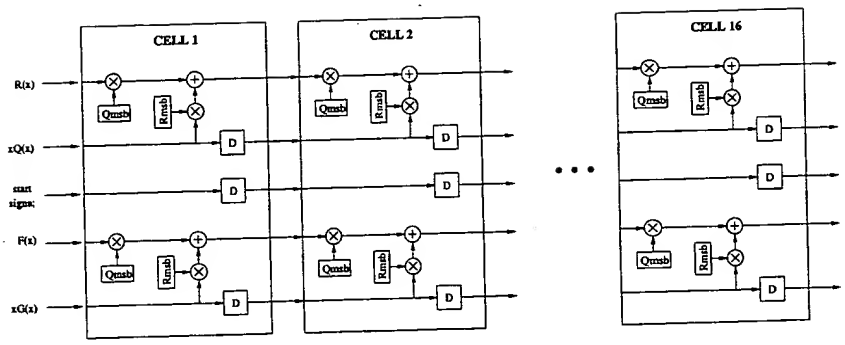


FIG. 8 (PRIOR ART)

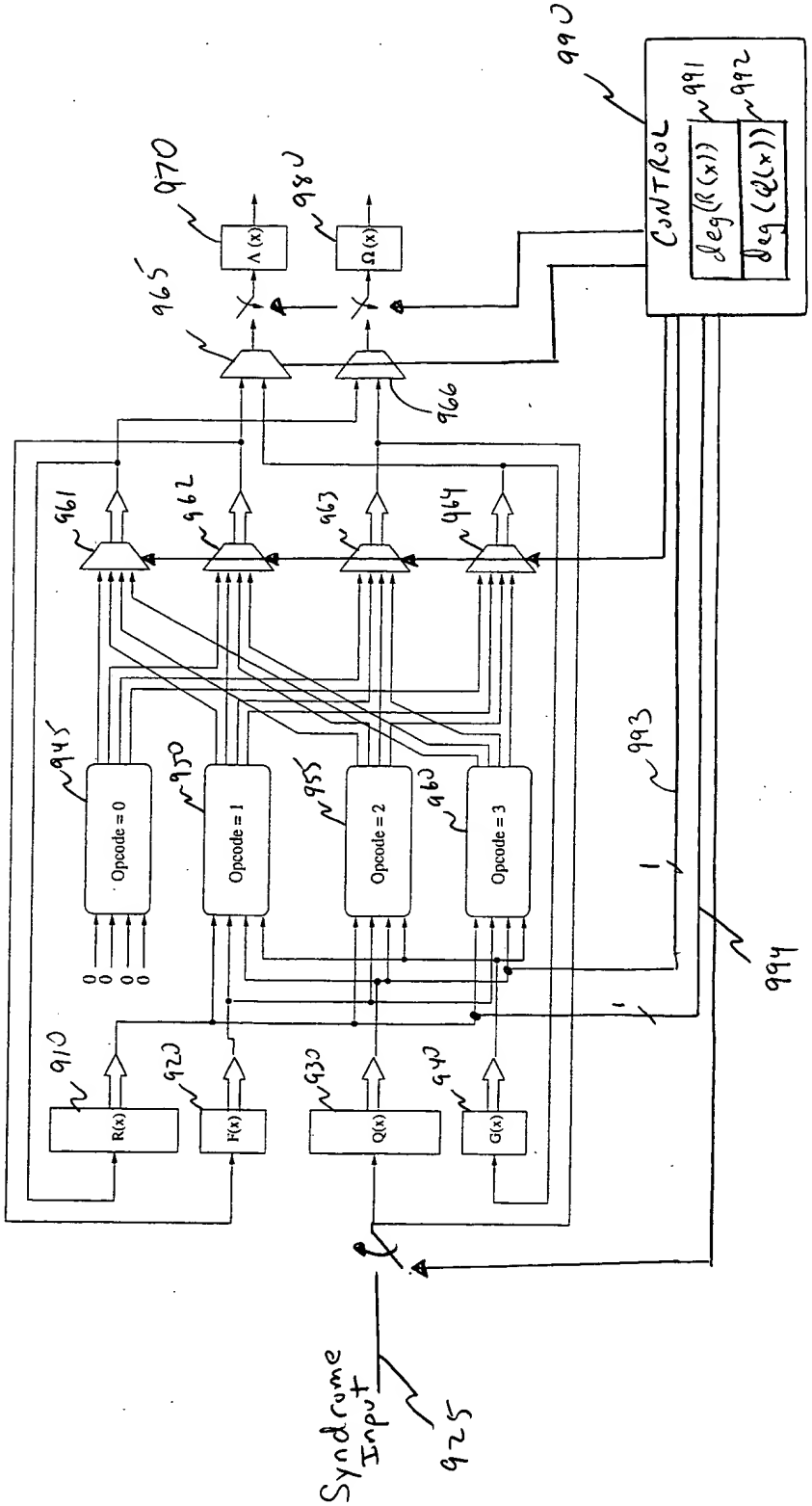

900
910
920
930
940
945
950
955
960
961
962
963
964
965
966
970
980
990
991
992
993
994
925
R(x)
F(x)
Q(x)
G(x)
Opcode = 0
Opcode = 1
Opcode = 2
Opcode = 3
Λ(x)
Ω(x)
CONTROL
deg(R(x))
deg(Q(x))
Syndrome Input

FIG. 9

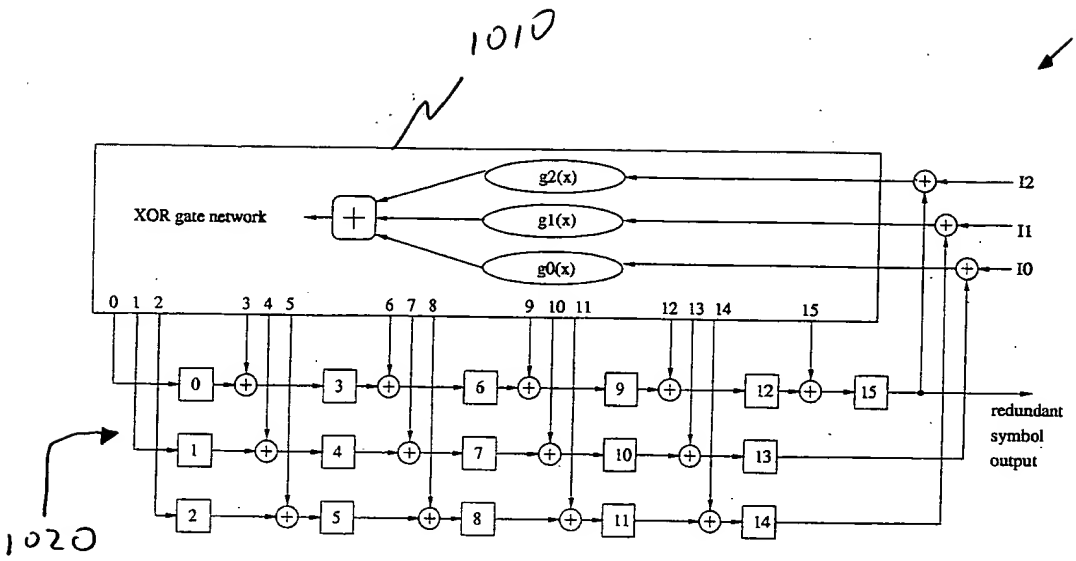


FIG. 10(a)

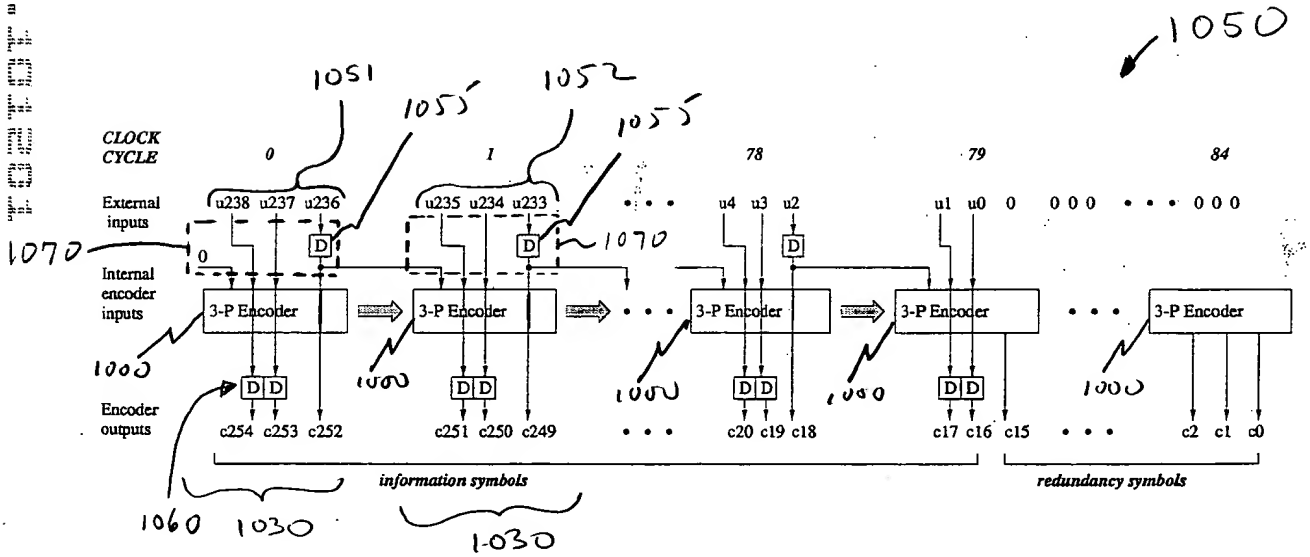


FIG. 10(b)

1100

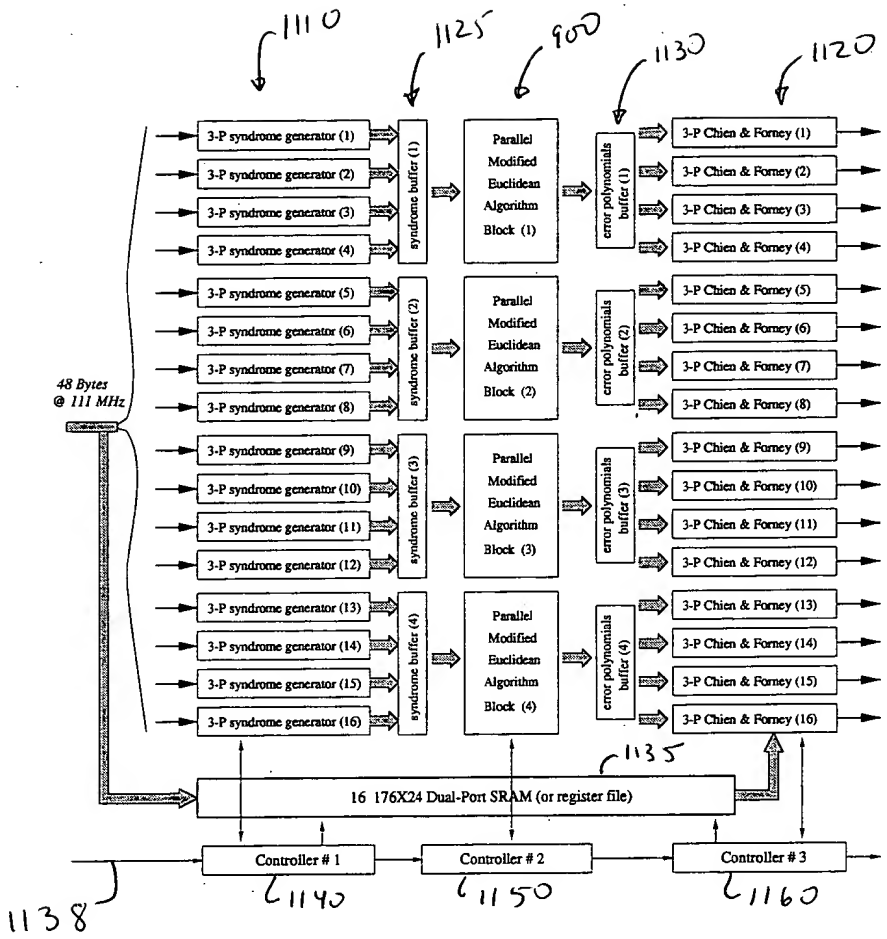
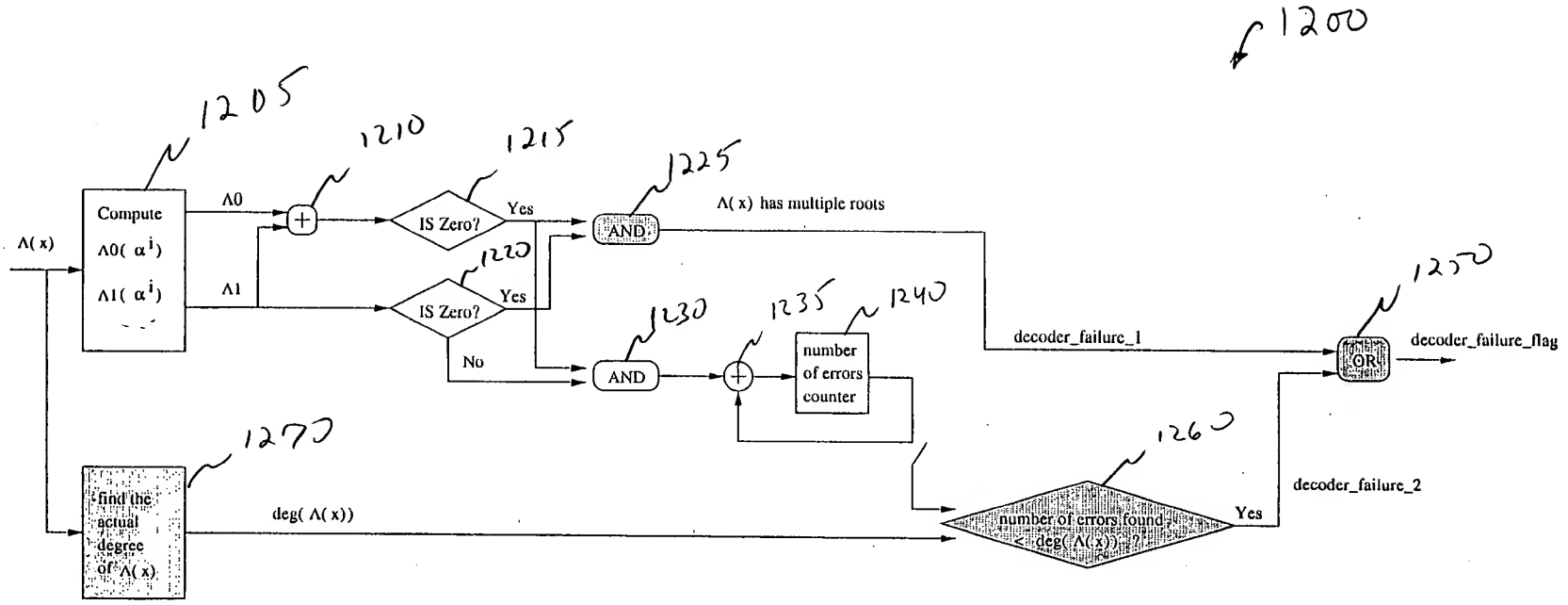

1110
1125
900
1130
1120
48 Bytes
@ 111 MHz
3-P syndrome generator (1)
3-P syndrome generator (2)
3-P syndrome generator (3)
3-P syndrome generator (4)
syndrome buffer (1)
Parallel Modified Euclidean Algorithm Block (1)
error polynomials buffer (1)
3-P Chien & Forney (1)
3-P Chien & Forney (2)
3-P Chien & Forney (3)
3-P Chien & Forney (4)
3-P syndrome generator (5)
3-P syndrome generator (6)
3-P syndrome generator (7)
3-P syndrome generator (8)
syndrome buffer (2)
Parallel Modified Euclidean Algorithm Block (2)
error polynomials buffer (2)
3-P Chien & Forney (5)
3-P Chien & Forney (6)
3-P Chien & Forney (7)
3-P Chien & Forney (8)
3-P syndrome generator (9)
3-P syndrome generator (10)
3-P syndrome generator (11)
3-P syndrome generator (12)
syndrome buffer (3)
Parallel Modified Euclidean Algorithm Block (3)
error polynomials buffer (3)
3-P Chien & Forney (9)
3-P Chien & Forney (10)
3-P Chien & Forney (11)
3-P Chien & Forney (12)
3-P syndrome generator (13)
3-P syndrome generator (14)
3-P syndrome generator (15)
3-P syndrome generator (16)
syndrome buffer (4)
Parallel Modified Euclidean Algorithm Block (4)
error polynomials buffer (4)
3-P Chien & Forney (13)
3-P Chien & Forney (14)
3-P Chien & Forney (15)
3-P Chien & Forney (16)
1135
16 176X24 Dual-Port SRAM (or register file)
Controller # 1
Controller # 2
Controller # 3
1140
1150
1160
1138

FIG. 11

TOSTOT"TE294650



F IG. 12

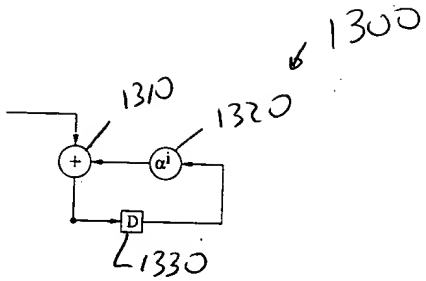


FIG. 13(a)

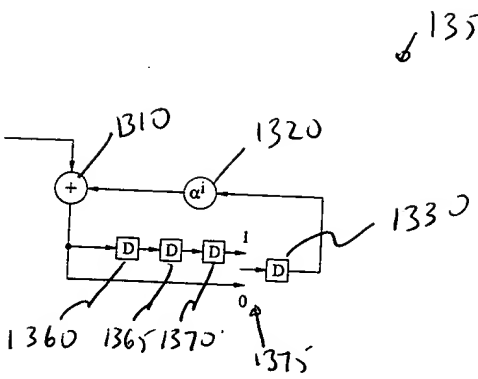


FIG. 13(b)

1400

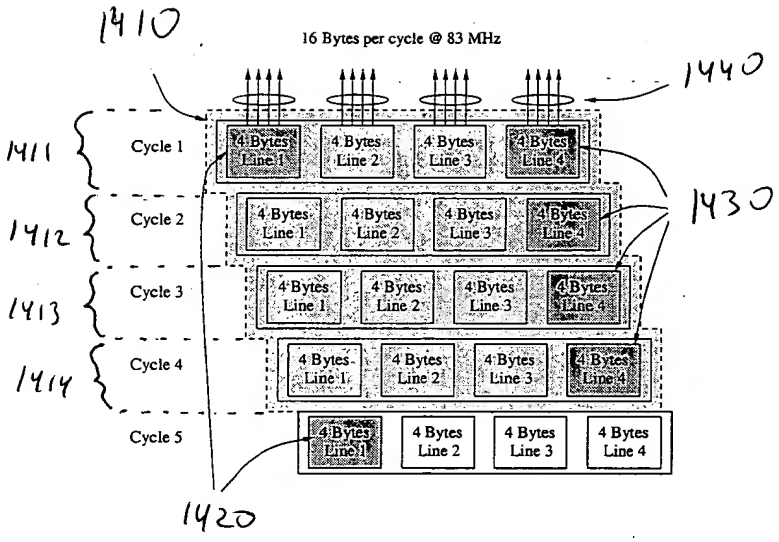

1410
16 Bytes per cycle @ 83 MHz
1440
1411
Cycle 1
1412
Cycle 2
1413
Cycle 3
1414
Cycle 4
Cycle 5
1430
4 Bytes Line 1
4 Bytes Line 2
4 Bytes Line 3
4 Bytes Line 4
1420

FIG. 14

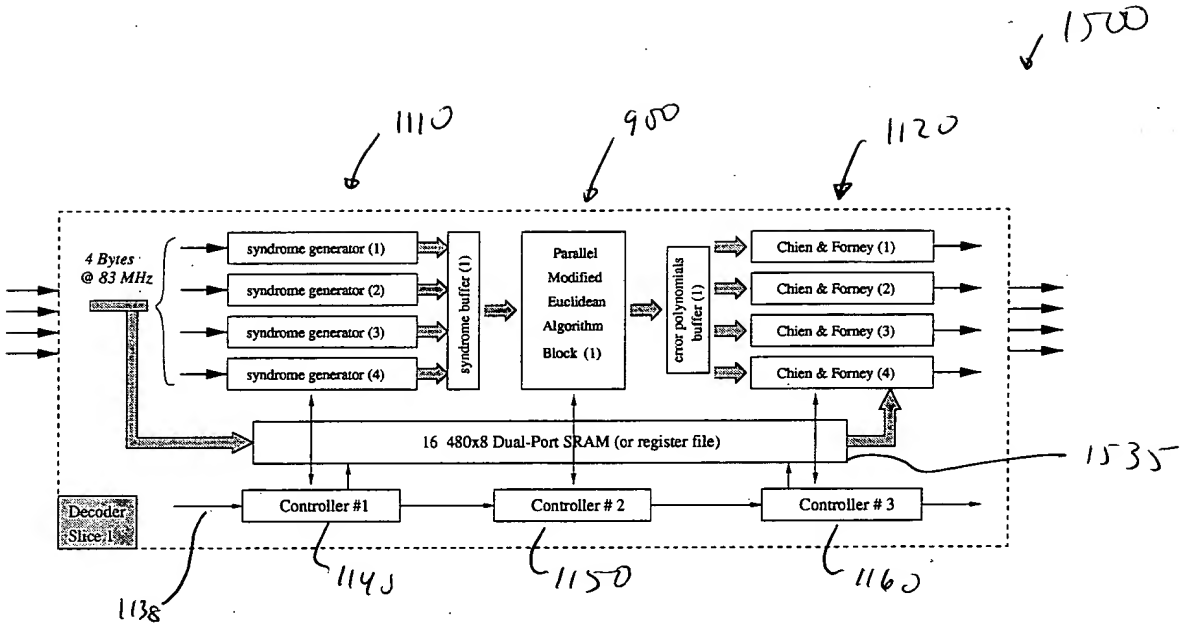
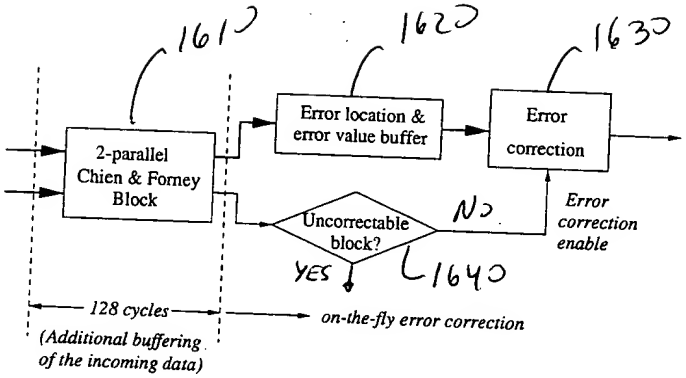

1500
1110
900
1120
4 Bytes
@ 83 MHz
syndrome generator (1)
syndrome generator (2)
syndrome generator (3)
syndrome generator (4)
syndrome buffer (1)
Parallel
Modified
Euclidean
Algorithm
Block (1)
error polynomials
buffer (1)
Chien & Forney (1)
Chien & Forney (2)
Chien & Forney (3)
Chien & Forney (4)
16 480x8 Dual-Port SRAM (or register file)
1535
Decoder
Slice 1
Controller #1
Controller # 2
Controller # 3
1138
1145
1150
1160

FIG. 15

1600


1610
1620
1630
2-parallel Chien & Forney Block
Error location & error value buffer
Error correction
Uncorrectable block?
NO
YES
1640
Error correction enable
128 cycles
(Additional buffering of the incoming data)
on-the-fly error correction